AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A double-gate field effect transistor ~~semiconductor device~~, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar.

2. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said strained-silicon channel thickness is substantially uniform.

3. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said strained-silicon channel thickness is set by epitaxial growth.

4. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said strained-silicon channel is substantially defect-free.

5. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said strained-silicon channel includes a distorted lattice cell.

6. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said first gate and said second gate are independently controllable.

7. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said strained-silicon channel comprises a fin.

8. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said first gate and said second gate are self-aligned.

9. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said first gate and said second gate are defined in a single lithographic step.

10. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said first gate, said second gate, said source and said drain are self-aligned with respect to each other.

11. (Currently Amended) The ~~device~~ transistor of claim 7, further comprising a plurality of fins.

12. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said device includes a planarized top surface.

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Original) A double-gate field effect transistor, ~~semiconductor device~~, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel comprises a fin.

22. (Currently Amended) A circuit, comprising:

the ~~semiconductor device~~ double-gate field effect transistor of claim 1.

23. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said strained-silicon channel is tensely strained.

24. (Currently Amended) The ~~device~~ transistor of claim 1, wherein said strained-silicon channel is compressively strained.

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Currently Amended) The ~~device~~ transistor of claim 1, wherein the first gate is electrically separated from the second gate.

29. (Currently Amended) The ~~device~~ transistor of claim 21, wherein the first gate is electrically separated from the second ~~gater~~ gate.

30. (Prviously Presented) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first sidewall of said channel;

a second gate formed over a second sidewall of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar, and said first and second sidewalls are opposing to each other.

31. (Previously Presented) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel, wherein said strained-silicon channel is non-planar, and is fixed to the substrate by said first and second gates.

32. (Currently Amended) The ~~device~~ transistor of claim 1, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor.

33. (Currently Amended) The ~~device~~ transistor of claim 21, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor.

34. (New) The transistor of claim 1, wherein said strained-silicon channel is controlled by said first gate and by said second gate.

35. (New) The transistor of claim 21, wherein said strained-silicon channel is controlled by said first gate and by said second gate.